the input sets of predecoded lines coupled to or communicating with the global x-decoders. While only, one set of lines **2807** are illustrated, mores sets (one set coupled to each local predecoder **2822** for example) are contemplated. The global predecoders **2820** ships out or transmits one or more signals on one set of the global predecoded lines and address inputs for each of the local predecoders **2822**.

[**0224**] Block Redundancy

[**0225**] Incorporating redundancy into memory structures to achieve reasonable higher yields in large memories is known. There are generally two main approaches to implementing such redundancy. First, it is known to replace the entire failing rows or columns. This approach is used when the partitioned memory subblocks are large, and where inserting extra rows and columns does not adversely effect area overhead.

[**0226**] However, when the partitioned memory subblocks are very small, the added rows and columns may make the entire row/column replacement approach less area effective and therefore less attractive. In such instances, it may be more effective to replace the entire block rather than replace specific rows or columns in the block. Known schemes for replacing blocks is generally accomplished using top level address mapping. However, top level address mapping may incur access time penalties.

[**0227**] The present invention relates to replacing small blocks in a hierarchically partitioned memory by either shifting the predecoded lines or using a modified shifting predecoder circuit in the local predecoder block. Such block redundancy scheme, in accordance with the present invention, does not incur excessive access time or area overhead penalties, making it attractive where the memory subblock size is small.

[**0228**] FIG. **29** illustrates one embodiment of a block diagram of a local predecoder block **3000**, comprising four local predecoders, **3000**A, **3000**B, **3000**C, **3000**D and one extra, inactive or redundant predecoder **3000**E. It is contemplated that, while four local predecoders and one extra predecoder are illustrated, more or less predecoders (for example five local predecoders and two extra predecoders, six local predecoders and one extra decoder, etc.) are contemplated. A plurality of predecoded lines are illustrated, which in one embodiment are paired together as inputs to one or more global x-decoders, forming the mapping from the row address inputs to the physical rows. In this embodiment, there are as many groups of predecoded lines as there are global inputs to the global decoder. For example, in one embodiment, there are two or three groups of precoded lines, although any number of predecoded line groups is contemplated.

[**0229**] In the illustrated embodiment, two predecoded line groups are illustrated, comprising higher address predecoded line group **3010** and lower address predecoded line group **3012**. The lower address predecoded line group **3012** acts similar to the least significant bit of a counter. The least significant predecoded line from a higher address predecoded line group **3010** is paired with at least one predecoded line from a lower address predecoded line group **3012**. More specifically, the least significant predecoded line from the higher address predecoded line group **3010** is paired with each and every predecoded line from a lower address precoded line group **3012**. This means that the predecoded lines from the higher address predecoded line group map to a contiguous number of rows in the memory cells. In one embodiment, the predecoded lines from the higher address predecoded line group map to as many rows as the number of predecoded lines in the lower address predecoded line group.

[**0230**] In one embodiment of the present invention, each block is selected by at least one line (or by predecoding a group lines) in the higher address predecoded line group. A higher address predecoder line shifts only if the shift pointer points to the particular redecoder line or the previous line has shifted.

[**0231**] FIG. **30** illustrates an unused predecoded line **3102** (similar to the predecoded lines in groups **3010** and **3012** provided previously) set to inactive in accordance with one embodiment of the present invention. This embodiment includes an associated fuse pointer **3104**. As illustrated, the fuse pointer **3104** is adapted to move or shift in only one direction (the right for example), such that the predecoded line **3102** is inactive if the fuse pointer is not shifted. Please note that while the fuse pointer as illustrated is adapted to shift in only one direction, other embodiments are contemplated, including having the fuse pointer shift in two or more directions, shift up and down, etc.

[**0232**] FIGS. **31**A & **31**B illustrate one embodiment of a local predecoder block **3200** similar to the predecoder **3000** in FIG. **29**. In this embodiment, predecoder block **3200** comprises four local (active) predecoders **3200**A, **3200**B, **3200**C, **3200**D and one extra or redundant predecoder **3200**E. A plurality of predecoded lines are illustrated, which in this embodiment, are again paired together as inputs to one or more global decoders, forming the mapping from the row address inputs to the physical rows.

[**0233**] In this embodiment, the illustrated predecoded lines comprise a plurality of predecoded lines **3202**A, **3202**B, **3202**C and **3202**D (similar to the unused predecoded line **3102** of FIG. **30**), which are set too inactive (i.e., not shifted). In this embodiment, predecoded lines **3202**A, **3202**B, **3202**C and **3202**D communicate with or are coupled to local (active) predecoders **3200**A, **3200**B, **3200**C and **3200**D respectively. Predecoded line **3202**E is coupled to the extra or redundant predecoder **3200**E. Furthermore, as illustrated, a plurality of fuse pointers **3204**A, **3204**B, **3204**C and **3204**D are associated with predecoded lines **3202**A, **3202**B, **3202**C and **3202**D respectively, where each fuse pointer is adapted to shift in only one direction. While only four predecoded lines, four fuse pointers and five predecoders are illustrated, any number and arrangement of lines, pointers and predecoders are contemplated.

[**0234**] By employing redundancy-shifting techniques to the higher predecoded line group, the rows are shifted in and out of the accessible part of the address space. Enabling shifting the rows provides a repair mechanism where a defective bit may be shifted out to the unused part of the address space. FIG. **31**B illustrates a defective predecoder (predecoder **3200**C for example) that is shifted out, such that that predecoder becomes inactive. In this embodiment, fuse pointer **3204**C shifts from predecoder line **3202**C to predecoder line **3202**D. Fuse shifter **3204**D shifts from predecoder line **3202**D to predecoder line **3202**E. In this manner,